



Webinar

On

“VLSI – Standard Cell Design”

- Date: 24th May 2020
- Resource Person: Mr. G. Prashanth Reddy Team lead, Intel India, Bangalore
- Platform: Zoom Meeting, ID: 87541324699
- Objective :
 - To enlight the students with basic VLSI Standard Cell Design
 - To provide a better understanding of Cell Design & Issues related as per the need of industry
- No. of participants: 113
- Target Participants: Students of 4th and 6th semester of ECE department.
- Outcome of the event: The Students gained knowledge on
 - Basics of VLSI & Cell Designs.
 - Timing Analysis of Memory Cells, Latency, Pipelining.
 - Obtained a practical exposure on VLSI Design.
 - Various Job Opportunities VLSI Industries.

“VLSI – Standard Cell Design”

RAJARAJESWARI COLLEGE OF ENGINEERING
 DEPT. OF ELECTRONICS & COMMUNICATION ENGINEERING

Webinar
 on
"VLSI- A Standard Cell Design"

FREE REGISTRATION
 Registration Link: <https://forms.gle/RB9jsabz7jCzQZ8>

Admissions Open 2020

Mr. Prashanth Reddy,
 Functional Safety Architect,
 Intel India Pvt Ltd,
 Bangalore

DATE: 24 MAY 2020
TIME: 11 AM TO 12:30 PM

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 Zoom ID: 8754124699
 Password: 708041

certificates will be provided

Standard cell Design

Gadila Prashanth Reddy

About Author

Gadila Prashanth Reddy
 Dr. Thesis dissertation in Intel India PVT Ltd

John Rules

- Standard cell design
- VLSI design expertise - PCB
- PMIC electrical validation Engineer
- SoC architecture - Functional Safety

Research Advisor: Ph.D. & Postdoc
 Guest Lectures: VIT university, RREC Bangalore, SVEC Nellore, SREC Anantapur, TRR Hyderabad, True VLSI, Sayarath Embedded systems, Gantapali Nellore and Sri Venkateswara Engineering Colleges

Patents & Publications
 International Patent Submissions
 International Patent Submissions
 "An Approach for Detection of Gas Leakage", India Patent number: 2019419037B9, Publication number: 2019419037B9
 "Single Chip Multi-Die Architecture Having Cross-Monitoring Capability", Publication number: 20190204125

International Journal and Conference publications
 Title: Estimation of Failure Rate in Bus-Voltage Resistor, Publication: Published as an article in Journal - IJITE (International Journal of recent Technology and Engineering) in Volume 5, Issue 258 - link: <https://www.ijite.org/issue/view/5258-258>
 Title: Multi Approach to Perform Dependent Failure Analysis in Compliance with Functional Safety Standards", Publication: Published in Springer proceedings in 7th International Conference on Computational Intelligence and Informatics (ICCI 2018), Link: <https://www.springer.com/9789811514724>
 Title: Assessing Functional Safety Parameters with respect to safety application, Publication: "International Journal of Advance Science and Technology" received acceptance and publication in process.
 Title: "Achieving ISO 26262 EC 61508 objectives with a common development process", Publication: "Published in Taylor and Francis conference proceedings in

Today's Topic

11:04 AM 7.4KB/s 4G

Close Participants (59)

Search

	Sumitha Manoj (me)			
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	Daphne (co-host)			
	Prashanth Reddy (co-host)			
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Invite

11:04 AM

Press [Esc] to exit full screen

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HOD/ECE